Technical Product Summary

Classic/PCI Pentium™ CPU Baby-AT Motherboard

Models:

BP5D60AT

Preliminary Version 0.1
April, 1993

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Preliminary Technical Product Summary
Revision 0.1

Table of Contents

Introduction

The Classic/PCI Pentium CPU Baby-AT Motherboard delivers excellent, cost effective performance in an industry standard, highly expandable Baby-AT form factor. A powerful Pentium™ Processor provides the horsepower for this high performance machine. Additionally, by incorporating a second level, high performance cache and four SIMM sites for memory expansion to 128 MB, five ISA expansion connectors and three PCI connectors, the Classic/PCI Pentium CPU Baby-AT Motherboard is ideally featured for expandable, performance sensitive desktop applications. A performance upgrade socket allows for easy upgrade in the field.

The Classic/PCI Pentium CPU Baby-AT Motherboard will excel in entry level Pentium Processor desktop PCs running existing compatible applications, as well as open up new markets due to it's workstation level performance.

BABY-AT FORM FACTOR

The Classic/PCI Pentium CPU Baby-AT motherboard matches the Baby-AT standards well established in the PC industry. This standard specifies the maximum board size, board mounting locations, and connector locations for the keyboard connector, as well as expansion slot placement. The Classic/PCI Pentium CPU Baby-AT meets all of these capabilities while adding PCI expansion possibilities. Figure 1 illustrates the Baby-AT form factor. A list of several chassis suppliers supporting the Baby-AT standard is included in the Appendices.

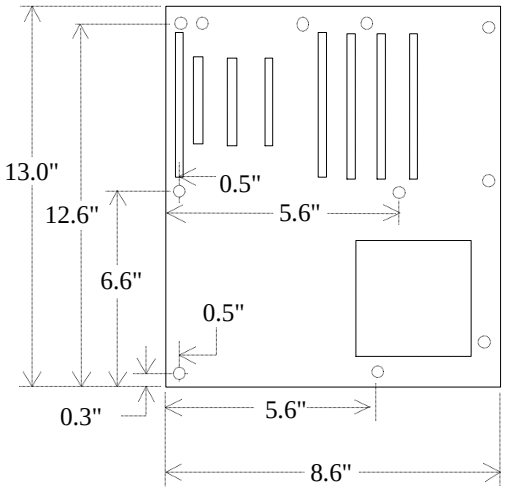


Figure 1. Classic/PCI Pentium CPU Baby-AT Motherboard dimensions.

Board Level Features

CPU

The Classic/PCI Pentium CPU Baby-AT Motherboard is designed to operate with a 66 MHz Pentium CPU, although the standard configuration uses a 60 MHz CPU for better desktop price/performance. Common features of the CPU include backward compatibility with the 8086, 80286, i386™ and i486™ CPUs, burst mode bus cycles, and an on-chip 16 KB cache. The cache is split into an 8K code cache and an 8K data cache which uses a write-back policy. The Pentium CPU contains a state of the art on-chip numeric coprocessor to significantly increase the speed of floating point operations, while maintaining backward compatibility with i486 DX math coprocessor and complying to ANSI/IEEE standard 754-1985.

PERFORMANCE UPGRADE

The primary CPU site includes a Zero Insertion Force socket which allows users to upgrade the CPU performance of their systems. An OverDrive processor is being developed for use with this socket which will provide enhanced performance over the Pentium processor. Since there is a Jumper (J3) on the motherboard that allows for CPU speed selection, an upgrade for a 60 MHz primary CPU can operate at a bus speed of 66 MHz.

SECOND LEVEL CACHE

In addition to the Pentium CPU's internal cache, the Classic/PCI Pentium CPU Baby-AT Motherboard provides a 256 KB external cache. Organized as direct mapped, write back architecture, this cache is implemented with eight 32K x 8 15 ns SRAM devices. The tag and control logic is contained in the 82434LX PCMC core chip.

SYSTEM BIOS

The Classic/PCI Pentium CPU Baby-AT Motherboard uses American Megatrends Incorporated (AMI) Pentium CPU ROM BIOS, which provides ISA compatibility. The system BIOS is stored in FLASH EEPROM, providing easy upgradability of program code space from a floppy disk or a file downloaded from a BBS; BIOS upgrades will be available for download from iPAN, the electronic bulletin board service of IntelTechDirect™. In addition to the AMI BIOS, the FLASH memory also contains the PCI Auto-configuration utility, SETUP utility, Power-On Self-Tests (POST), and update recovery code. For improved system performance, the Classic/PCI Pentium CPU Baby-AT Motherboard supports system BIOS shadowing, allowing the BIOS to execute from 32-bit on-board write-protected DRAM instead of the slower 8-bit FLASH devices.

The Classic/PCI Pentium CPU Baby-AT BIOS sign-on during POST is along the bottom of the screen, and contains information which identifies revision and type of BIOS. On the lower left is a four digit code which denotes revision; first production units will display 0101, and as updates occur will roll the "minor revision number", i.e. 0102. BIOS level and board identifier code is contained on the lower right side, and will be P00.AE0 for the Classic/PCI i486 Baby-AT motherboard. As a note, A01 denotes Alpha revision 01, and B01 denotes Beta revision 01.

Further information on BIOS functions can be found in the IBM PS/2 and Personal Computer BIOS Technical Reference published by IBM, and the ISA and EISA Hi-Flex AMIBIOS Technical Reference published by AMI and available at most technical bookstores.

PCI AUTO-CONFIGURATION CAPABILITY

The PCI Auto-configuration feature provides a new level of user satisfaction. Simply plug a PCI add-in card into an empty connector and turn the system on. The BIOS automatically configures interrupts, DMA channels, I/O space, etc. No requirement for additional jumper changes because of potential resource conflicts provides unrivaled ease of use in a PC.

The auto-configuration routine operates in conjunction with an ISA configuration utility. This utility enables the user to specify the ISA options used, and ties into the PCI configuration software transparently to provide seamless add-in card installation.

SETUP UTILITY

Classic/PCI Pentium CPU Baby-AT incorporates many commonly used system setup features into the FLASH EEPROM. The BIOS SETUP Program has been enhanced and provides several new options to take advantage of the Classic/PCI Pentium CPU Baby-AT Motherboard's new features. New options include:

- Auto configuration of IDE hard disks.
- Support for four IDE disk drives (primary and secondary)
- Cache/Shadow Memory Option -- Provides the user the option to assign a block of addresses below the 1 MB boundary as non-shadowed, non-cached. Primarily used for expansion card ROM which causes timing issues when shadowed and cached.
- ISA interrupts - Allows ISA interrupts IRQ9, IRQ10, IRQ15 to be assigned to add-in ISA adapters, thereby informing the PCI configuration utility which interrupts not to use.
- Cache/Shadow Memory Option -- Provides the user the option to assign a block of addresses below the 1 MB boundary as non-shadowed, non-cached. Primarily used for expansion card ROM which cause timing issues when shadowed and cached.

The setup utility is accessible only during the Power-On Self Test by pressing the <F1> key anytime after the POST memory test has begun and before boot begins. For security purposes, access to SETUP can be disabled via a jumper on the motherboard. The ROM-based setup allows the system configuration to be modified without opening the system for most basic changes. Setup options are detailed in Appendix C.

FLASH IMPLEMENTATION

The Intel 28F001BXT 1 Mb FLASH component is organized as 128K x 8 (128 KB). The Flash device is divided into five areas, as described in Table 2.

System Address		*FLASH Memory Area*
F0000H	FFFFFH	64 KB Main BIOS
EE000H	EFFFFH	8 KB Boot Block (Not FLASH erasable)
ED000H	EDFFFH	4 KB Parameter Block (used for PCI)
EC000H	ECFFFH	4 KB Flash User Area
E0000H	EBFFFH	System BIOS

Table 1. Flash Memory Organization

The FLASH device resides in system memory in two 64 KB segments starting at E0000H, and is distributed in two different organizations, depending on the mode of operation. In *Normal Mode* address line A16 is inverted, switching the E000H and F000H segments so that the BIOS is organized as shown in the system address column above. *Recovery mode* removes the inversion on address line A16, swapping the E000H and F000H segments so that the 8 KB boot block resides at FE000H where the i486 expects the bootstrap loader to exist. This mode is only necessary in the unlikely event that a BIOS upgrade procedure is interrupted, causing the BIOS area to be left in an unusable state. For information on recovering the BIOS in the event of a catastrophic failure, refer to Appendix D.

UPGRADE UTILITY

FLASH memory brings new opportunities for distributing BIOS upgrades. Installing a new version of BIOS will no longer require removal of the system cover and the replacement of EPROM's. Instead, the upgrade can be done completely from a floppy diskette. Easy access to BIOS upgrades will be available through down-loadable files on the iPAN bulletin board.

Security is provided in two ways. First, the FLASH upgrade utility insures the upgrade BIOS matches the target system to prevent accidentally installing a BIOS for a different type of system. Second, security to prevent unauthorized changes to the BIOS is provided via a write protect jumper on the motherboard. The default setting is to allow BIOS upgrades. A recovery jumper is provided to recover from the unlikely event of an unsuccessful BIOS upgrade. It forces the ROM decode to access a 32 KB block of write protected code in the FLASH device that facilitates recovery. The default value for this jumper is for "normal" mode (note: this jumper is not changed during normal BIOS updates, it is used only if a problem is encountered).

The disk-based FLASH upgrade utility (FMUP.EXE; download able from iPAN) has three options for BIOS upgrades:

- The FLASH BIOS can be updated from a file on a disk;
- The current BIOS code can be copied from the FLASH EEPROM to a disk file as a backup in the event that an upgrade cannot be successfully completed; and
- The BIOS in the FLASH device can be compared with a disk file to ensure the system has the correct BIOS version.

FLASH USER AREA

Classic/PCI Pentium CPU Baby-AT supports a 4 KB programmable Flash User area located at ED00-EDFF. A programmer may use this area to display a customized message or to execute a small program. The Classic/PCI Pentium CPU Baby-AT BIOS accesses the user area just after completing the POST (Power-On Self-Test) if the setup option is enabled. The flash user area may be updated by running the FMUP.EXE utility, which expects the update files to have a .USR extension. Sample programs and instructions are in the file CLSUSER.ZIP on the iPAN bulletin board.

KEYBOARD (AND MOUSE) INTERFACE

An Intel 8742 surface mount micro controller contains the Phoenix Technologies compatible keyboard/mouse controller code. An AT style keyboard connectors is located on the back panel side of the motherboard. The 5V line on this connector is protected with a PolySwitch® circuit which acts much like a fuse except that it re-establishes the connection after an over-current condition is removed. While the PolySwitch eliminates the possibility of having to replace a fuse, care should be taken to turn the system power off before installing or removing a keyboard. As a manufacturing option, customers whose chassis will allow two PS/2 style connectors, one for mouse and one for keyboard, can be supported by offering PS/2 configuration instead of AT. The 8742 micro controller code supports Power-On/Reset (POR), network, and keyboard password protection. Network and keyboard passwords require programs contained on the utility disk that ships with the system, the POR password is set via the SETUP program. In addition, the keyboard controller provides for the following "HOT" key sequences:

- CTRL-ALT-DEL: System software reset. This sequence performs a software reset of the system by jumping to the beginning of the BIOS code and running the POST operation, excluding memory tests.
- <TBD 1> and <TBD 2>: Turbo mode selection. <TBD 1> sets the system for de-turbo mode (emulation of an 8 MHz 80286 CPU using wait states) and <TBD 2> sets the system for turbo mode (its normal operation at 60 MHz or 66 MHz). Changing the Turbo mode may be prohibited by an operating system or application software.

SYSTEM MEMORY

The Classic/PCI Pentium CPU Baby-AT Motherboard provides four 36-bit wide SIMM sites for memory expansion. The memory array is controlled by the Intel 82434LX PCMC, and data buffering is provided by two Intel 82433LX Local Bus eXtension devices. The four SIMM sites support 256K x 36, 512K x 36, 1M x 36, 2M x 36, 4M x 36 and 8M x 36 SIMM modules. Maximum memory size, using four 32M x 36 SIMM modules is 128 MB. Memory timing is designed for 70 ns fast page devices, faster DRAMs will operate in the board but will provide no performance improvement. Parity generation/checking is provided for each 8-bit byte.

SIMMs may be installed in combinations of two or four modules and each two SIMMs must be of the same memory size and type (see the Appendix for a complete list of combinations). These restrictions allow the memory design to be optimized for the best possible performance. There are no jumper settings required for the memory size configuration, the System BIOS automatically sizes memory and initializes the 82434LX DRAM controller for appropriate DRAM configuration.

CORE CHIP SET

The core chip set is the Intel Mercury chip set, consisting of one 82434LX PCI/Cache/Memory Controller (PCMC), two 82433LX Local Bus eXtension (LBX) devices, and one 82378IB System I/O (SIO) bridge chip. The Mercury chip set provides the following functions:

- CPU reset control
- CPU L1 cache control
- CPU burst mode control
- CPU interface control
- Integrated L2 write-back cache controller with tag comparator
- Page-mode DRAM controller
- Burst memory read/write control logic
- Data bus conversion to PCI
- Parity generation/detection to memory
- AT-BUS direction control
- Chip select for keyboard controller and RTC
- Speaker control
- NMI logic
- Floating-point coprocessor interface
- Keyboard reset and gate A20 emulation logic
- DMA controller
- Interrupt controller
- Counters/Timers

82434LX PCI/CACHE/MEMORY CONTROLLER (PCMC)

The 82434LX provides all control signals necessary to drive the DRAM array, including multiplexed address signals. It also controls system access to memory and generates snoop controls to maintain cache coherency.

82433LX LOCAL BUS EXTENSION (LBX)

The 82433LX provides data bus buffering and dual port buffering to the memory array. Controlled by the 82434LX, the 82433LX devices add one load each to the PCI bus and perform all the necessary byte and word swapping required. Memory and I/O write buffers are included in these devices.

82378IB SYSTEM I/O (SIO)

The 82378IB integrates seven 32-bit DMA channels, five 16-bit timer/counters, two eight-channel interrupt controllers, NMI logic, refresh address generation, and PCI/ISA bus arbitration circuitry together onto the same device.

EXPANSION SLOTS

The Classic/PCI Pentium CPU Baby-AT Motherboard contains support for up to seven populated expansion slots, including ISA and PCI connectors. These connectors include four ISA bus expansion slots, and three PCI expansion slot; the seventh slot uses both an ISA connector and a PCI connector side by side, and can accept either an ISA or PCI adapter board but not both together. The expansion cards are oriented perpendicular to the motherboard. All three PCI expansion slots accept PCI master cards to fully support the PCI specification.

DALLAS DS12887 REAL TIME CLOCK, CMOS RAM AND BATTERY

The Real Time Clock (RTC) is implemented using a Dallas DS12887 device. The DS12887 is accurate to within 13 minutes/year and requires no external support (the battery and oscillator are integrated into the device). The component is socketed and can be replaced if the internal battery loses its charge (the internal battery has an estimated lifetime of ten years).

The RTC can be set via the BIOS SETUP Program. CMOS memory supports the standard 128-byte battery-backed RAM, fourteen bytes for clock and control registers, and 114 bytes of general purpose non-volatile CMOS RAM. All CMOS RAM is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program. Also, the CMOS RAM values can be cleared to the system defaults by using a hardware jumper. Appendix B lists jumper configurations.

FRONT PANEL CONNECTORS

A connector (J3A1) is provided for installing a speaker. The speaker provides error beep code information during the Power-On Self Test if the system cannot use the video interface. The Classic/PCI Pentium CPU Baby-AT product guide contains beep and error code information.

Connectors J1G1, J1G2, J1I1, and J1H1, J1H2 supply front panel connections to Reset, Key lock, and Turbo switches, and hard disk and turbo LEDs, respectively.

SCSI SUBSYSTEM

NCR 53C810 SCSI I/O PROCESSOR (SIOP)

The on-board SCSI I/O processor is a NCR 53C810. This component has internal FIFOs on the SCSI and PCI busses, supporting 32-bit address and data, and an internal SCRIPTS processor capable of fast mastering DMA over PCI. The SIOP runs at 33 MHz and supports PCI burst mode, the maximum theoretical data transfer rate is 132 MB/sec across the PCI bus, and 10 MB/sec across the Fast SCSI bus.

SCSI PHYSICAL INTERFACE

The SCSI Physical Interface consists of the 50-pin header connectors for internal routing to SCSI peripherals, Fats SCSI termination at the beginning of the SCSI bus, the SCSI termination power circuitry, and jumpers to enable the feature.

A ribbon cable should be used to connect the baseboard SCSI bus to the SCSI hard drive. The Classic/PCI Pentium CPU Baby-AT supports only the single ended SCSI mode. By setting jumper J13F1 and J13F2 to 2-3, on-board SCSI is enabled. Setting these jumpers to 1-2 disables this feature.

Up to seven SCSI devices can be connected via a ribbon cable. The connector is placed on the motherboard to optimize routing of the cable. For allowing external expansion of SCSI, the cable must end with a SCSI connector attached to a metal plate, which is then inserted into the empty slot opening on the back of the Baby-AT chassis.

The SCSI standard requires termination at each end of the bus. The on-board bus is terminated at the beginning, therefore termination must be provided at the final device on the SCSI daisy chain. Termination for the internal final device must have termination resistors installed only if the cable will not provide an external SCSI connection. If the cable routes to an eternal connector, an external termination block must be installed (unless an external device is connected). These termination blocks are available from many sources. The on-board termination is the active termination required for Fast SCSI-II. 5V termination power is routed to pin 26 of the header connector through a PolyFuse circuit.

SCSI DRIVERS

SCSI drivers for DOS are shipped with the system. No drivers are required for DOS if Protected Mode of the CPU is not used i.e. memory mangers or Windows 3.1 is NOT used, and the only peripheral devices installed are SCSI hard disks using the onboard SCSI controller: All functions are taken care of by the SCSI BIOS. All other situations, such as multiple host adapters, mixture of SCSI and IDE drives, booting from a SCSI device other than a hard drive, use of an extended memory manager (such as QEMM, EMM386 or Windows 3.1), etc., require installation of the supplied SCSI drivers. Please see the Appendices for a complete matrix of driver information.

SECURITY

Security features are incorporated into the Classic/PCI Pentium CPU Baby-AT system BIOS.

BIOS PASSWORD

A BIOS password feature provides security during the boot process. A password can be entered using the Setup utility and must be re-entered prior to disk boot each time the system is reset. The password can be changed at the password prompt by entering <old password> / <new password> / <new password> <enter>. The password also can be cleared by entering <old password> / <enter>. If the password is forgotten, it can be cleared by turning off the system and setting jumper J9I4 to 2-3. After the system has finishes the Power-On Self Test, turn the system off and

reset jumper J9I4 to 1-2. This allows the user to again access the password feature, but with the forgotten password cleared.

SETUP ENABLE JUMPER

A jumper on the baseboard controls access to the BIOS Setup utility. By setting jumper J9I1 to 2-3, the user is prevented from accessing the Setup utility during the Power-On Self Test or at any other time.

System Integration Features

BACK PANEL CONNECTIONS

The back panel provides external access to the keyboard controller integrated on the Classic/PCI Pentium CPU Baby-AT motherboard. Figure 4 shows the back panel connection.

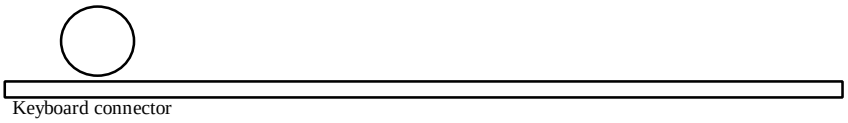


Figure 2. Classic/PCI Pentium CPU Baby-AT Back panel

POWER SUPPLY

The Classic/PCI Pentium CPU Baby-AT board could be powered by a 200 watt switch able power supply, providing power for onboard resources, add-in cards, and peripherals.

DC Voltage	*Max. Continuous Current*	*Peak Current 15 Seconds*	*Minimum Current Load*
+5V	18.5A	18.5	2.5A
-5V	0.9A	0.9A	0A
+12V	4.6A	9.5A	0.5A
-12V	0.5A	0.5A	0A

Table 2. Classic/PCI Pentium CPU Baby-AT Current Requirements

Table 2 lists the current used by system resources. This information is preliminary and is provided only as a guide for calculating approximate total system power usage with additional resources added.

Resource	*Typical Power*
Classic/PCI Pentium CPU Baby-AT baseboard, 16 MB (8 MB in each of two banks), 256K cache	50 Watts
Teac 3½" Floppy drive	1.7 Watts

Table 3. Current Use by System Resources (Preliminary)

Appendices

APPENDIX A - USER-INSTALLABLE UPGRADES

SYSTEM MEMORY

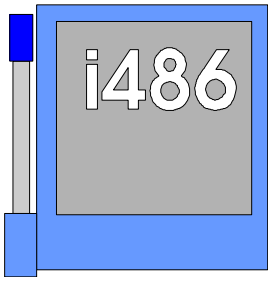
Table A-1 shows the total system memory based on the listed combinations of SIMMs in the two banks.

SIMM 1,2 (Bank 0) SIMM Type (Amount)	*SIMM 3,4 (Bank 1) SIMM Type (Amount)*	*Total System Memory*
256K X 36 (1 MB)	Empty	**2 MB**
256K X 36 (1 MB)	256K X 36 (1 MB)	4 MB
256K X 36 (1 MB)	512K X 36 (2 MB)	6 MB
256K X 36 (1 MB)	1M X 36 (4 MB)	10 MB
256K X 36 (1 MB)	2M X 36 (8 MB)	18 MB
256K X 36 (1 MB)	4M X 36 (16 MB)	34 MB
256K X 36 (1 MB)	8M X 36 (32 MB)	66 MB
512K X 36 (2 MB)	Empty	4 MB
512K X 36 (2 MB)	256K X 36 (1 MB)	6 MB
512K X 36 (2 MB)	512K X 36 (2 MB)	8 MB
512K X 36 (2 MB)	1M X 36 (4 MB)	12 MB
512K X 36 (2 MB)	2M X 36 (8 MB)	20 MB
512K X 36 (2 MB)	4M X 36 (16 MB)	36 MB
512K X 36 (2 MB)	8M X 36 (32 MB)	68 MB
1M X 36 (4 MB)	Empty	8 MB
1M X 36 (4 MB)	256K X 36 (1 MB)	10 MB
1M X 36 (4 MB)	512K X 36 (2 MB)	12 MB
1M X 36 (4 MB)	1M X 36 (4 MB)	16 MB
1M X 36 (4 MB)	2M X 36 (8 MB)	24 MB
1M X 36 (4 MB)	4M X 36 (16 MB)	40 MB
1M X 36 (4 MB)	8M X 36 (32 MB)	72 MB
2M X 36 (8 MB)	Empty	16 MB
2M X 36 (8 MB)	256K X 36 (1 MB)	18 MB
2M X 36 (8 MB)	512K X 36 (2 MB)	20 MB
2M X 36 (8 MB)	1M X 36 (4 MB)	24 MB
2M X 36 (8 MB)	2M X 36 (8 MB)	32 MB
2M X 36 (8 MB)	4M X 36 (16 MB)	48 MB
2M X 36 (8 MB)	8M X 36 (32 MB)	80 MB
4M X 36 (16 MB)	Empty	32 MB
4M X 36 (16 MB)	256K X 36 (1 MB)	34 MB
4M X 36 (16 MB)	512K X 36 (2 MB)	36 MB
4M X 36 (16 MB)	1M X 36 (4 MB)	40 MB
4M X 36 (16 MB)	2M X 36 (8 MB)	48 MB
4M X 36 (16 MB)	4M X 36 (16 MB)	64 MB
4M X 36 (16 MB)	8M X 36 (32 MB)	96 MB
8M X 36 (32 MB)	Empty	64 MB
8M X 36 (32 MB)	256K X 36 (1 MB)	66 MB
8M X 36 (32 MB)	512K X 36 (2 MB)	68 MB
8M X 36 (32 MB)	1M X 36 (4 MB)	72 MB
8M X 36 (32 MB)	2M X 36 (8 MB)	80 MB
8M X 36 (32 MB)	4M X 36 (16 MB)	96 MB
8M X 36 (32 MB)	8M X 36 (32 MB)	**128 MB**

Table A-1. Possible SIMM Memory Combinations

PERFORMANCE UPGRADE

An OverDrive processor will be available for the OverDrive components are available from Intel's Personal Computer Enhancement Division. For the location of the nearest Intel dealer, phone 1 (800) 538-3373.



Just Look for the Blue ZIF Socket!

QUALIFIED DRAM SIMMS

Vendor	*Part Number*	*Size (configuration)*
Toshiba	THM361010AS-70	
Toshiba	THM361020AS-70	
Samsung	KMM5361000A-7	
Samsung	KMM5361000B-7	
Hitachi	HB56D136SBS-7A	
Micron	MT9D136M-7	
MTI	Z124MBK36A-70I1	
MTI	Z124MBK36B-70I1	
MTI	Z124MBK36R-70IN	

Table A-2. Sampling of memory DRAM SIMM Vendors

APPENDIX B - JUMPERS

(* denotes default setting)

J1I2 - SET CPU SPEED

Note: Use J1I2 only for a speed change when installing an upgrade processor. Changing the speed of the main processor can damage the component.

	J1I2
60 MHz	2-3
66 MHz	1-2

Table B-1. CPU speed select options.

J13F1, J13F2 - ENABLE SCSI

	J13F1	*J13F2*
Enable	2-3	2-3
Disable	1-2	1-2

Table B-2. SCSI enable/disable Options.

J8I2 - FLASH BOOT BLOCK (RECOVERY MODE ENABLE)

1-2	Recovery mode boot	2-3*	Boot from standard BIOS

J8I1 - CLEAR CMOS JUMPER

1-2*	Don't clear CMOS	2-3	Clear CMOS upon power-up

J9I1 - CMOS SETUP PROTECTION

1-2*	Allow user to enter Setup	2-3	Prevent user from entering Setup

J9I2 - FLASH WRITE

2-3*	Disable +12V to FLASH	1-2	Enable +12V to FLASH (Erasable)

J9I3 - COLOR/MONO

1-2	Monochrome mode video	2-3*	Color mode video

J9I4 - PASSWORD JUMPER

1-2*	Enable password	2-3	Disable and clear password

APPENDIX C - SETUP OPTIONS

TBD

APPENDIX D - BIOS RECOVERY

The Classic/PCI Pentium CPU Baby-AT incorporates an AMI system BIOS on a FLASH component. FLASH BIOS allows easy upgrades without the need to replace an EPROM. The upgrade utility fits on a floppy diskette and provides the capability to save, verify, and update the system BIOS. The upgrade utility can be run from a hard drive or a network drive, but no memory managers can be installed during upgrades.

The latest upgrade utility and BIOS code are available in the *public* section of the iPAN bulletin board.

USING THE UPGRADE UTILITY

If the utility is obtained from iPAN, UNZIP the archive and copy the files to a bootable MS-DOS 3.3, 4.01, 5.0, or 6.0 bootable diskette. Reboot the system with the upgrade diskette in the bootable floppy drive and follow the directions in the easy to use menu-driven program.

RECOVERY MODE

In the unlikely event that a FLASH upgrade is interrupted catastrophically, it is possible the BIOS may be left in an unusable state. Recovering from this condition requires the following steps (be sure a power supply has been attached to the board, and a floppy drive is connected as drive A:):

1. Change jumper J8I2 to position 1-2.
2. Install the bootable upgrade diskette into drive A:
3. Reboot the system.
4. Because of the small amount of code available in the non-erasable boot block area, no video is available to direct the procedure. The procedure can be monitored by listening to the speaker and looking at the floppy drive LED. When the system beeps and the floppy drive LED is lit, the system is copying the recovery code into the FLASH device. As soon as the drive LED goes off, the system can be turned off.
5. Reset jumper J8I2 to position 2-3.
6. Leave the upgrade floppy in drive A: and turn the system on.
7. Continue with the original upgrade.

APPENDIX E - MEMORY MAP

Address Range (Deci-	*Address Range (hex)*	*Size*	*Description*
16384K-32768K	1000000-2000000	16384K	Extended Memory
16256K-16383K	FE0000-FFFFFF	128K	System & Video BIOS Copy
1024K-16255K	100000-FDFFFF	15232K	Extended Memory
960K-1023K	F0000-FFFFF	64K	AMI System BIOS
952K-959K	EE000-EFFFF	8K	FLASH Boot Block (Available as HIMEM)
948K-951K	ED000-EDFFF	4K	User FLASH Area (available as HIMEM if no user info is here)
928K-947K	E8000-ECFFF	20K	AMI Setup Program (disable via setup pre-boot only; with this
896K-927K	E0000-E7FFF	32K	Video BIOS (when installed)
800K-895K	C8000-DFFFF	96K	Available Hi DOS Memory(open to the ISA bus)
768K-799K	C000-C7FFF	32K	Optional VGA BIOS
736K-767K	B8000-BFFFF	32K	VGA Display Memory (not available to ISA bus)
704K-735K	B0000-B7FFF	32K	VGA & Mono Display Memory (HIMEM w/ QEMM)(not available to
640K-703K	A0000-AFFFF	64K	VGA Display Memory (not available to the ISA bus)
639K	9FC00-9FFFF	1K	Extended BIOS Data (moveable by QEMM, 386MAX)
512K-638K	80000-9FBFF	127K	Extended conventional
0K-511K	00000-7FFFF	512K	Conventional

Table E-1. Classic/PCI Pentium CPU Baby-AT Memory Map

APPENDIX F - I/O MAP

Address Range (hex)	*Size (Decimal)*	*Description*
0000 - 000F	16 bytes	SIO - DMA 1
0020 - 0021	2 bytes	SIO - Interrupt Controller 1
0040 - 0043	4 bytes	SIO - Timer 1
0048 - 004B	4 bytes	SIO - Timer 2
0060	1 byte	Keyboard Controller Data Byte
0061	1 byte	SIO - NMI, speaker control
0064	1 byte	Keyboard Controller, CMD & STATUS Byte
0070, bit 7	1 bit	SIO - Enable NMI
0070, bits 6:0	7 bits	SIO - Real Time Clock, Address
0071	1 byte	SIO - Real Time Clock, Data
0073	1 byte	Reserved - Board Configuration
0075	1 byte	Reserved - Board Configuration
0078	1 byte	SIO - BIOS Timer
0080 - 008F	16 bytes	SIO - DMA Page Register
00A0 - 00A1	2 bytes	SIO - Interrupt Controller 2
00C0 - 00DE	31 bytes	SIO - DMA 2
00F0	1 bytes	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
0278 - 027B	4 bytes	Parallel Port 2
02F8 - 02FF	8 bytes	On-Board Serial Port 2
0376	1 byte	Secondary IDE Channel Command Port
0377	1 byte	Secondary IDE Channel Status Port
0378 - 037F	8 bytes	Parallel Port 1
03BC - 03BF	4 bytes	Parallel Port x
03E8 - 03EF	8 bytes	Serial Port 3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 bytes	Primary IDE Channel Command Port
03F7 (Write)	1 byte	Floppy Channel 1 Command
03F7, bit 7	1 bit	Floppy Disk Change Channel 1
03F7, bits 6:0	7 bits	Primary IDE Channel Status Port
03F8 - 03FF	8 bytes	On-Board Serial Port 1
0CF8	1 byte	PCI Configuration Space Enable
0CF9	1 byte	Deturbo Mode Enable
C000 - C0FF	256 bytes	82434LX Configuration Registers
C200 - C2FF	256 bytes	82378IB Configuration Registers

Table F-1. Classic/PCI i486 Baby-AT I/O Address Map

APPENDIX G - BOARD INTERRUPTS & DMA

Interrupt Request	*System Resource*
NMI	Parity Error
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Parallel Port 2
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	User available
10	User available
11	User available
12	On-board Mouse Port if enabled, else user available
13	Reserved, Math coprocessor
14	IDE if enabled
15	User available

Table G-1. Classic/PCI i486 Baby-AT Interrupt Map

DMA Channel	*Data Width*	*System Resource*
0	8- or 16-bits	Open
1	8- or 16-bits	Open - Normally used for LAN
2	8- or 16-bits	Floppy
3	8- or 16-bits	IDE
4		Reserved - Cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

Table F-3. Classic/PCI i486 Baby-AT DMA Map

APPENDIX H - CONNECTORS

AT STYLE KEYBOARD PORT (J13H1 = KEYBOARD)

Pin Number	Signal Name
1	Clock
2	Data
3	No Connect
4	Ground
5	Vcc (fused)

Table H-1. AT Style Keyboard Connector Pin Definition

OPTIONAL PS/2 STYLE KEYBOARD, MOUSE PORTS (J13H2 = KEYBOARD, J13I1 = MOUSE)

Pin Number	Signal Name
1	Data
2	No Connect
3	Ground
4	Vcc (fused)
5	Clock
6	No Connect

Table H-2. PS/2 Mouse and Keyboard Connector Pin Definition

PRIMARY POWER CONNECTOR (J11I1)

Pin	Name	Function
1	PWRGD	Power Good
2	+5 V	+ 5 volts Vcc
3	+12 V	+ 12 volts
4	-12 V	- 12 volts
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	-5 V	-5 volts
10	+5 V	+ 5 volts Vcc
11	+5 V	+ 5 volts Vcc
12	+5 V	+ 5 volts Vcc

Table H-3. Power Connector Pin Definition

AUXILIARY (3.3V) POWER CONNECTOR (J10I1)

Pin	Name	Function
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	+3.3 V	+ 3.3 volts
5	+3.3V	+ 3.3 volts
6	+3.3 V	+ 3.3 volts

Table H-4. 3.3V Power Connector Pin Definition

SPEAKER CONNECTOR (J3A1)

Pin Number	Signal Name
1	SPKR DAT
2	Key
3	No Connect
4	+5V Vcc

Table H-5. Speaker Connector Pin Definition

AUXILIARY 12V FAN CONNECTOR (J1A1)

Pin Number	*Signal Name*
1	Ground
2	+12V (fused)
3	Ground

Table H-6. 12V Fan Connector Pin Definition

RESET CONNECTOR (J1G1)

Pin Number	*Signal Name*
1	RESET
2	Ground

Table H-7. Reset Switch Connector Pin Definition

KEY LOCK/POWER LED CONNECTOR (J1G2)

Pin Number	*Signal Name*
1	LED_PWR
2	Key
3	Ground
4	KEY LOCK
5	Ground

Table H-8. Key lock / Power LED Connector Pin Definition

HARD DRIVE LED CONNECTOR (J1H1)

Pin Number	*Signal Name*
1	PULL_UP_330
2	HD ACTIVE-
3	Key
4	PULL_UP_330

Table H-9 Fixed Disk LED Connector Pin Definition

TURBO LED CONNECTOR (J1H2)

Pin Number	*Signal Name*
1	PULL_UP_330
2	LED_TURBO-

Table H-10. Turbo LED Connector Pin Definition

TURBO SWITCH CONNECTOR (J1I1)

Pin Number	*Signal Name*
1	TURBO
2	Ground
3	No Connect

Table H-11. Turbo Switch Connector Pin Definition

ISA CONNECTORS (J6G2, J6G1, J5G1, J4G1, J1G1)

Signal Name	*Pin Number*	*Pin Number*	*Signal Name*
GND	B1	A1	IOCHK-
RSTDRV	B2	A2	SD7
Vcc	B3	A3	SD6
IRQ9	B4	A4	SD5
-5V	B5	A5	SD4
DRQ2	B6	A6	SD3
-12V	B7	A7	SD2
0WS-	B8	A8	SD1
+12V	B9	A9	SD0
GND	B10	A10	IOCHRDY
SMEMW-	B11	A11	AEN
SMEMR-	B12	A12	SA19
IOW-	B13	A13	SA18

IOR-	B14	A14	SA17
DACK3-	B15	A15	SA16
DRQ3	B16	A16	SA15
DACK1-	B17	A17	SA14
DRQ1	B18	A18	SA13
REFRESH-	B19	A19	SA12
SYSCLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DACK2-	B26	A26	SA5
TC	B27	A27	SA4
BALE	B28	A28	SA3
Vcc	B29	A29	SA2
OSC	B30	A30	SA1
GND	B31	A31	SA0
	KEY	KEY	
MEMCS16-	D1	C1	SBHE-
IOCS16-	D2	C2	LA23
IRQ10	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
DACK0-	D8	C8	LA17
DRQ0	D9	C9	MEMR-
DACK5-	D10	C10	MEMW-
DRQ5	D11	C11	SD8
DACK6-	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7-	D14	C14	SD11
DRQ7	D15	C15	SD12
Vcc	D16	C16	SD13
Master-	D17	C17	SD14
GND	D18	C18	SD15

Table H-12. ISA Connector Pin Definition

PCI CONNECTORS (J3H1, J2H1, J1H1)

Signal Name	*Pin Number*	*Pin Number*	*Signal Name*
GND	A1	B1	-12V
+12V	A2	B2	TCK
No Connect	A3	B3	GND
STDI	A4	B4	STD0
Vcc	A5	B5	Vcc
PCIINT3-	A6	B6	Vcc
PCIINT1-	A7	B7	PCIINT2-
Vcc	A8	B8	PCIINT4-
Reserved	A9	B9	No Connect
Vcc	A10	B10	Reserved
Reserved	A11	B11	No Connect
GND	A12	B12	GND
GND	A13	B13	GND

Reserved	A14	B14	Reserved
SPCIRST-	A15	B15	GND
Vcc	A16	B16	PCLKE
AGNT-	A17	B17	GND
GND	A18	B18	REQA-
Reserved	A19	B19	Vcc
AD30	A20	B20	AD31
3.3V	A21	B21	AD29
AD28	A22	B22	GND
AD26	A23	B23	AD27
GND	A24	B24	AD25
AD24	A25	B25	3.3V
AD22 (IDSEL)	A26	B26	CBE3-
3.3V	A27	B27	AD23
AD22	A28	B28	GND
AD20	A29	B29	AD21
GND	A30	B30	AD19
AD18	A31	B31	3.3V
AD16	A32	B32	AD17
3.3V	A33	B33	CBE2-
FRAME-	A34	B34	GND
GND	A35	B35	IRDY-
TRDY-	A36	B36	3.3V
GND	A37	B37	DEVSEL-
STOP-	A38	B38	GND
3.3V	A39	B39	PLOCK-
SDONE	A40	B40	PERR-
SBO-	A41	B41	3.3V
GND	A42	B42	SERR-
PAR	A43	B43	3.3V
AD15	A44	B44	CBE1-
3.3V	A45	B45	AD14
AD13	A46	B46	GND
AD11	A47	B47	AD12
GND	A48	B48	AD10
AD9	A49	B49	GND
key	A50	B50	key
key	A51	B51	key
CBE0-	A52	B52	AD8
3.3V	A53	B53	AD7
AD6	A54	B54	3.3V
AD4	A55	B55	AD5
GND	A56	B56	AD3
AD2	A57	B57	GND
AD0	A58	B58	AD1
Vcc	A59	B59	Vcc
SREQ64-	A60	B60	SACK64-
Vcc	A61	B61	Vcc
Vcc	A62	B62	Vcc

Table H-13. PCI Connector Pin Definition

OPTIONAL SCSI CONNECTOR (J29)

Signal Name	*Pin Number*	*Pin Number*	*Signal Name*
Ground	1	2	Data 0
Ground	3	4	Data 1
Ground	5	6	Data 2
Ground	7	8	Data 3
Ground	9	10	Data 4
Ground	11	12	Data 5
Ground	13	14	Data 6
Ground	15	16	Data 7
Ground	17	18	Parity
Ground	19	20	Ground
Ground	21	22	Ground
Ground	23	24	Ground
No Connect	25	26	Termination Power
Ground	27	28	Ground
Ground	29	30	Ground
Ground	31	32	Attention
Ground	33	34	Ground
Ground	35	36	Busy
Ground	37	38	Acknowledge
Ground	39	40	Reset
Ground	41	42	Message
Ground	43	44	Select
Ground	45	46	CD
Ground	47	48	Request
Ground	49	50	I/O

Table H-14. Optional SCSI Connector Pin Definition

APPENDIX I - BABY-AT CHASSIS SUPPLIERS

Axxion Group Corporation
11 B. Leigh Fisher
El Paso, TX 79906
(915) 772-0088

Enlight Corporation, USA
345 Cloverleaf Drive, Unit 2B
Baldwin Park, CA 91706
(818) 369-4709

Olsen Metal Products
1001 Crossroads Boulevard
Seguin, TX 78155
(512) 379-2799

Suntek Corporation
xxx
xxx
(xxx) xxx-xxxx

Kepro Corporation
xxxx
xxx
(xxx) xxx-xxxx

APPENDIX J - ENVIRONMENTAL STANDARDS

Parameter	*Condition*	*Specification*
Temperature		
	Non-Operating	-40ºC to +70ºC
	Operating	+0ºC to +55ºC
Humidity		
	Non-Operating	92% Relative Humidity max. @ 36ºC
	Operating	80% Relative Humidity max. @ 36°C
Altitude		
	Non-Operating	50,000 feet (15,240 meters)
	Operating	10,000 feet (3048 meters)
ESD		
	1.0kV	No Errors
	2.5kV	No Errors
	5.0kV	5% Soft Errors, 0% Hard Errors, No physical damage
	7.5kV	10% Soft Errors, 0% Hard Errors, No physical damage
	10.0kV	25% Soft Errors, 5% Hard Errors, No physical damage
	12.5kV	50% Soft, 10% Hard, No physical damage
	15.0kV	100% Soft, 25% Hard, No physical damage
	25.0kV	100% Soft, 100% Hard, No physical damage
Shock	Non-Operating	30.0G, 11ms, 1/2 sine

Table J-1. Environmental Standards

APPENDIX K - RELIABILITY DATA

This Mean-Time-Between-Failures (MTBF) data is calculated from predicted data @ 55C.

Classic/PCI Pentium CPU Baby-AT baseboard (BP5D60AT8C) xx,xxx hours

APPENDIX L - CUSTOMER SUPPORT

The Classic/PCI Pentium CPU Baby-AT is backed by Intel's industry-leading support groups in the OEM Products and Services Division (OPSD), including IntelTechDirect™. OPSD can support many of your network integration and service needs, including worldwide integration and system repair services. IntelTechDirect provides the following 4 major services:

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An electronic Bulletin board with current product information, demo software and more...

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- FLASH BIOS upgrade files
- Modem set at no parity, 8 data bits, 1 stop bit.

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- Hardware and software compatibility notes
- Documentation updates, spare parts and order information

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- Information on End-of-Life products
- Available worldwide through direct dial at 916-356-3105

For information about IntelTechDirect please contact your local Intel Sales Representative.

APPENDIX M - PHYSICAL DIMENSIONS

BOARD

Length	32.8 cm	13.0"
Width	21.8 cm	8.6"

Table J-1. Motherboard Outline Dimensions

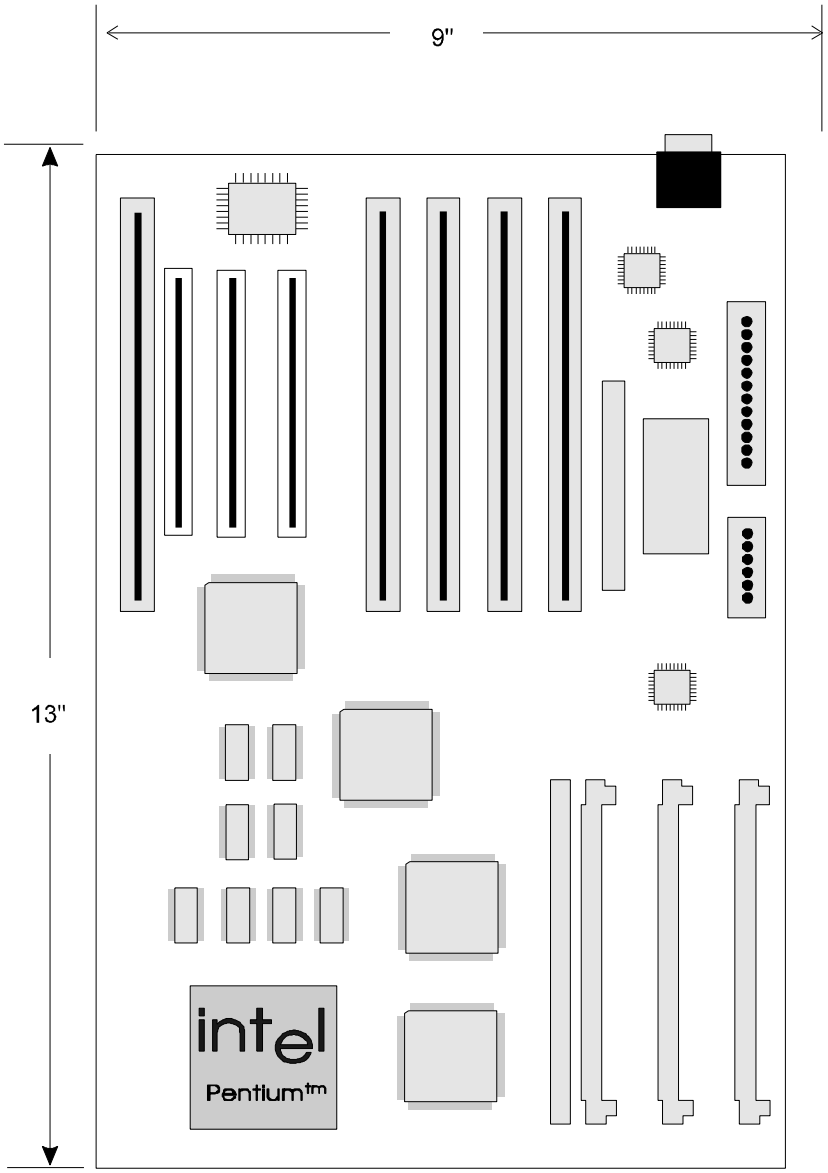

Figure J-1. Classic/PCI Pentium CPU Baby-AT Motherboard Dimensions

APPENDIX N - PRODUCT CODES

BOARDS

BP5D60AT8C	Classic/PCI Pentium CPU Baby-AT, 8 MB, 256K Cache
BP5D60AT8CS	Classic/PCI Pentium CPU Baby-AT, 8 MB, 256K Cache, SCSI Option

(All boards are bulk shipped in quantities of 10)

ACCESSORIES

Accessory kit includes:

DOCUMENTATION

The Classic/PCI Pentium CPU Baby-AT board ships with a product guide.